1st IEEE International Workshop on

CHIPLET INTERCONNECT TEST and REPAIR

in conjunction with IEEE European Test Symposium 2024
Thursday, May 23, 16:30-18:30h and Friday, May 24, 08:30-16:00h, 2024
https://ets24.nl/index.php/workshops/citar/

Call for Participation

The first IEEE International Workshop on Chiplet Interconnect Test and Repair (CITaR) focuses exclusively on the test and repair of interconnects for chiplet-based, three-dimensional stacked ICs, and the on-chip infrastructure which enables that. These ICs include so-called 2.5D-, 3D-, and 5.5D-stacked ICs. Die-to-die interconnects might contain micro-bump pairs, hybrid bonds, interposer wires, and through-silicon vias (TSVs). While these stacked ICs offer many attractive advantages with respect to heterogeneous integration, small form-factor, high bandwidth and performance, and low power dissipation, there are many open issues with respect to testing and repairing their inter-die interconnects. The CITaR Workshop offers a unique forum to present and discuss these challenges and (emerging) solutions among researchers and practitioners alike.

You are invited to participate in the CITaR Workshop. The CITaR Workshop will take place in conjunction with the IEEE European Test Symposium (ETS) in the Marriott Hotel in The Hague in the Netherlands and is technically sponsored by the Test Technology Technical Council (TTTC) of IEEE Computer Society.

Workshop Program – The workshop program contains the following elements.

- Keynote Address by Jeff Rearick, Senior Fellow at AMD (USA):
  "Stepping up to the Chiplet (Interconnect) Test Challenge"
- Five sessions encompassing 14 paper presentations, each concluded by a short panel with the speakers.
- Social functions: a welcome reception on Day 1 and a lunch on Day 2.

For the detailed version of the program, please see overleaf.

Participation – You are invited to participate in the workshop. Participation requires registration and a registration fee. Workshop registration includes access to all technical sessions, the Electronic Workshop Digest (containing extended abstracts, papers, slides, posters, as made available by their presenters), the welcome reception, coffee break, and lunch. On-line registration is available via the website of the IEEE European Test Symposium (https://ets24.nl/index.php/registration).

Key Dates & Deadlines • Workshop on-site registration: May 23+24, 2024

Further Information

General Chair:
Erik Jan Marinissen – imec
Kapeldreef 75
3001 Leuven, Belgium
erik.jan.marinissen@imec.be
Tel.: +32 16 28-8755

Program Chair:
Martin Keim – Siemens EDA
8005 SW Boeckman Rd
Wilsonville, OR 97070, US
martin.keim@siemens.com
Tel.: +1 503 685 7082

Publication Chair:
Adrian Evans – CEA/LIST
17 Rue des Martyrs
38054 Grenoble, France
adrian.evans@cea.fr
Tel.: +33 4 38 78 04 41

Publicity Chair:
Po-Yao Chuang – imec
Kapeldreef 75
3001 Leuven, Belgium
po-yao.chuang@imec.be
Tel.: +32 456-569099

Media Partners:

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Workshop Program

all times are Central European Summer Time (CEST)

Day 1: Thursday May 23, 2024

Session 1: Opening

Moderator: Jin-Fu Li – National Central University (TW)

16:30h: **Welcome Address**
General Chair: Erik Jan Marinissen – imec (BE)
Program Chair: Martin Keim – Siemens EDA (USA)

16:40h: **Keynote Address:**
Stepping up to the Chiplet (Interconnect) Test Challenge
Jeff Rearick – AMD (USA)

Abstract: Through some amazing advances in packaging technology, we've entered the "More-than-Moore" era where the long-predicted slowdown in chip density and performance not only didn't happen but went the other direction: assembling multiple chiplets into a single package has enabled gigantic transistor counts and staggering power levels that the test community must grapple with in new ways. This talk will review the latest technology trends (with examples from the industry), touch on some of the test challenges that come along with the entire chiplet ecosystem, then focus on the unique challenges of chiplet-to-chiplet interconnect test and repair. Topics will include 2.5D vs. 3D testing, soft vs. hard repair, standards, fault models, data volume, test access, partial assembly test, thermal management and power delivery, among others. The inescapable conclusion is that there is a substantial amount of hard work to do and that we test engineers will be in the spotlight to get it done.

17:25h: **Illuminating Blind Spots in Chiplet Interconnect Testing**
Nir Sever – Proteantecs (USA)*

17:50h: **DfT Standards Lessons for IEEE Std P3405**
Martin Keim – Siemens EDA (USA)*

18:15h: **Panel on Session 1**
All speakers

Welcome Reception

18:30h: **Welcome Reception**

19:30h: **End of Day 1**

Day 2: Friday May 24, 2024

Session 2: Interconnect and Repair

Moderator: Lori Schramm – Siemens EDA (USA)

08:30h: **Physical Aware Interconnect Testing and Repairing of Chiplets**
Tuanhui Xu – HiSilicon (CN)*

08:55h: **An Exploration of Error Correction Approaches for Chiplet Interfaces**
Antoine Rouget – ST Microelectronics (FR)*

09:20h: **Insights on Chip Repair Techniques from Existing Industrial Solutions**
Adrian Evans – CEA/LIST (FR)

09:50h: **Panel on Session 2**
All speakers

Coffee/Tea Break

10:00h: **Coffee/Tea Break**

Session 3: Related Topics

Moderators: Hans Martin von Staudt – Renesas (DE)

10:30h: **Interconnects in 3D Technology**
Jaber Derakhshandeh – imec (BE)*

10:55h: **The Reliability Imperative: Navigating Challenges in 3D IC Integration**
Stéphane Moreau – CEA/LETI (FR)*

11:20h: **Streamlining Silicon Photonic Chiplet Testing**
Quan Yuan – FormFactor (USA)*

11:45h: **Test and Repair of Small Bridging Defects Occurring to TSVs in a 3D-DRAM Using Enhanced Pulse-Vanishing Test**
Shi-Yu Huang - National Tsing-Hua University (TW)*

12:05h: **Panel on Session 3**
All speakers

Lunch

12:15h: **Lunch**

Session 4: IEEE Std P3405: Standard under Development

Moderator: Ivo Steverink – JTAG Technologies (NL)

13:30h: **Repair Logic Description Language**
Po-Yao Chuang, Erik Jan Marinissen – imec (BE)*

14:05h: **Examples of EDA Tools Based on a Standardized Repair Description Language**
Tsung-Hsuan Wang – imec/NYCU (BE/TW);*
Po-Yao Chuang, Erik Jan Marinissen – imec (BE)

14:40h: **IEEE Std P3405 from an EDA Vendor Point of View**
Martin Keim, Anshuman Chandra – Siemens EDA (USA)*

15:10h: **Panel on Session 4**
All speakers

Session 5: Closure

Moderator: Tibbe van der Biezen – Nederlands Forensisch Instituut (NL)

15:20h: **Introducing IEEE Std P3405 Chiplet Interconnect Test and Repair Standardization Effort**
Sreejit Chakravarty – Ampere Computing, Chair P3405 (USA)

Abstract: The chiplet revolution is upon us. It is revolutionizing the way we design, fabricate, and test large and feature-rich SoCs. This revolution will be greatly enhanced if chiplets from different vendors can be seamlessly packaged together and effectively tested. For better yield, repair must be factored in. This complex task cannot be effectively performed without a well-defined standard for test and repair. This talk will introduce the audience to the ongoing effort in standardizing the chiplet interconnect test and repair as part of IEEE P3405 standardization WG.

15:55h: **Farewell**
General Chair: Erik Jan Marinissen – imec (BE)

16:00h: **End of Day 2**

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