29th IEEE European Test Symposium (ETS) 2024

May 20-24, The Hague, Netherlands

ETS 2024 Full Program

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ETS Registration information

ETS conference	Registration desk at hotel lobby
Monday 20 May	12:00-18:30
Tuesday 21 May	08:00-18:30
Wednesday 22 May	08:00-15:00
Thursday 23 May	08:00-16:00

ETS workshop	Registration desk at hotel lobby
Thursday 23 May	16:00-18:00
Friday 24 May	08:00-08:30

Monday May 20th, 2024

14:00 – 18:30 TSS Tutorials @ ETS

The TSS Tutorials on Monday afternoon are free of charge for ETS24 registered attendees. The full TSS program can be found here.

Time	Room	Moderator	Session title and speaker
14:00 – 16:00	A1		***Tutorial 1: Silicon Fault Analysis (FA) equipment for security analysis*** Presenter: Jean-Pierre Seifert, *TU Berlin (DE)*
14:00 – 16:00	Van Gogh + Monet		***Tutorial 2: Security of Generative AI and Generative AI for Security*** Presenters: Ramesh Karri, *NYU, (US)* and Jeyavijayan (JV) Rajendran, *Texas A&M University (US)*
16:00 – 16:30	***Coffee Break***		
16:30 – 18:30	A1		***Tutorial 1: Silicon Fault Analysis (FA) equipment for security analysis*** Presenter: Jean-Pierre Seifert, *TU Berlin (DE)*
16:30 – 18:30	Van Gogh + Monet		***Tutorial 2: Security of Generative AI and Generative AI for Security*** *Presenters: Ramesh Karri, NYU, (US) and Jeyavijayan (JV) Rajendran, Texas A&M University (US)*

19:00 – 20:30 ETS24 Welcome Reception

Tuesday May 21st, 2024

09:00 – 12:30 Morning Session

Time	Room	Event	Session title and speaker
09:00 – 09:30	A1	*Conference Opening*	
09:30 – 10:15	A1	Keynote 1 Chair:	***Silent Data Corruption Errors in VLSI Circuits: Implications, Challenges, and Opportunities*** Speaker: Rama Govindaraju, Google (US) **Abstract**: VLSI chips are the foundation of our computing infrastructure and we all rely on it to function reliably. Trust of our users and the entire industry is at stake. There is increasing evidence of reliability issues with modern VLSI chips. The defect rates are orders of magnitude higher than what has traditionally been cited. Amplifying this challenge is the point that an increasing number of these chips are silently corrupting the execution context (or SDC - silent data corruption and is inconsistent with the expectation of a failstop model). We will also discuss the challenges emerging from degradation/aging. This discussion will summarize some of the experiences at Google and a sketch of what Google has been doing to address this growing challenge. We will attempt to increase awareness of the growing challenge and also the many opportunities for research to address this problem. The goal will be to make louder the call to action that Google has been championing for the last 5 years to enable an end to end solution that addresses this emerging and growing challenge for the entire computing industry. This is an industry wide problem and needs everyone to contribute to enable the solution space.
10:15 – 11:00	Basement	***Coffee Break – Scientific poster 1***	

10:15 – 11:00 Poster Session 1
Room - Basement

Poster 1: Formal Resilience Metric Characterization in Complex Digital Systems

Authors: *Damiano Zuccala[1,2], Jean-Marc Daveau[1], Philippe Roche[1], Katell Morin-Allory[2]*
[1]STMicroelectronics (FR)
[2]Univ. Grenoble Alpes, CNRS (FR)

Poster 2: Analyzing the Structural and Operational Impact of Hardware Faults in Floating-Point and Posit Arithmetic Cores for CNN Operations

Authors: *Josie Rodriguez Condia, Juan-David Guerrero-Balaguera, Robert Limas Sierra, Matteo Sonza Reorda*
Politecnico di Torino (IT)

Poster 3: Hardening Bus-Encoders with Power-Aware Single Error Correcting Codes

Authors*: Shlomo Engelberg[1], Osnat Keren[2]*
[1]Jerusalem College of Technology (IL)
[2]Bar-Ilan University (IL)

Poster 4: MBIST-based weak bit screening method for embedded MRAM

Authors: *Jongsin Yun[1], Sina Bakhtavari Mamaghani[3], Mehdi Tahoori[3], Christopher Muench[2], Martin Keim[1]*
[1]Siemens Digital Industries Software (US)
[2]Siemens Digital Industries Software (DE)
[3]Karlsruhe Institute of Technology (DE)

Poster 5: GNN-Based INC and IVC Co-optimization for Aging Mitigation

Authors: *Yu-Guang Chen[1], Hsiu-Yi Yang[1], Ing-Chao Lin[2]*
[1]National Central University (TW)

Poster 7: A Fully Pipelined High-Performance Elliptic Curve Cryptography Processor for NIST P-256

Authors: *Han Yan[1,2], Shuai Chen[3], Junying Huang[1,2], Jing Ye[1,2,4], Huawei Li[1,2,4], Xiaowei Li[1,2]*
[1]Institute of Computing Technology CAS (CN)
[2]University of Chinese Academy of Sciences (CN)
[3]Binary Semiconductor (CN)
[4]CASTEST co (CN)

Poster 8: Parallel-Check Trimming Test Approach for Selecting the Reference Resistance of STT-MRAMs

Authors*: Pei-Yun Lin, Jin-Fu Li*
National Central University (TW)

Poster 9: A Concept of Provably Detected Defects for Analog Defect Simulation Campaign Improvement

Authors: *Vladimir Zivkovic[1], Inga Abel[2], Anthony Candage[3]*
[1]Infineon Technologies (DK)
[2]Infineon Technologies (DE)
[3]Infineon Technologies (US)

Poster 10: A Multi-Objective Evolutionary Approach for Test Network Design

Authors: *Payam Habiby[1], Fatemeh Shirinzadeh[2], Sebastian Huhn[3], Rolf Drechsler[1,2]*
[1]University of Bremen (DE)
[2]DFKI (DE)
[3] Siemens Digital Industries Software (DE)

Poster 11: AdAM: Adaptive Fault-Tolerant Approximate Multiplier for Edge DNN Accelerators

Authors: *Mahdi Taheri[1], Natalia Cherezova[1], Samira Nazari[2], Ahsan Rafiq[1], Ali*

10:15 – 11:00 Poster Session 1
Room - Basement

[2]National Cheng Kung University (TW)

Azarpeyvand[1,2], Tara Ghasempouri[1], Masoud Daneshtalab[1,3], Jaan Raik[1], Maksim Jenihhin[1]
[1]Tallinn University of Technology (EE)
[2]University of Zanjan (IR)
[3]Malardalen University (SE)

Poster 6: Error Detection and Correction Codes for Safe In-Memory Computations

Authors: Luca Parrini[1,4], Taha Soliman[1], Benjamin Hettwer[1], Jan Micha Borrmann[1], Simranjeet Singh[2], Ankit Bende[2], Vikas Rana[2], Farhad Merchant[3], Norbert When[4]
[1]Bosch Corporate Research Robert Bosch GmbH (DE)
[2]Forschungszentrum Jülich (DE)
[3]Newcastle University (UK)
[4]RPTU Kaiserslautern-Landau (DE)

Poster 12: Training Large Language Models for System-Level Test Program Generation Targeting Non-functional Properties

Authors: Denis Schwachhofer[1], Peter Domanski[1], Steffen Becker[1], Stefan Wagner[1,2], Matthias Sauer[3], Dirk Pflueger[1], Ilia Polian[1]
[1]University of Stuttgart (DE)
[2]Technical University of Munich (DE)
[3]Advantest Europe (DE)

11:00 - 12:30 Parallel Sessions

Regular Session 1: Test Generation and Compression

Room: A1
Moderator:

Talk 1: Faulty Function Extraction for Defective Circuits

Authors: Chris Nigh[1], Purdy Ruben[1], Wei Li[1], Subhasish Mitra[2], Shawn Blanton[1]
[1]Carnegie Mellon University (US)
[2]Stanford University (US)

Talk 2: Time and Space Optimized Storage-based BIST under Multiple Voltages and Process Variations

Authors: Hanieh Jafarzadeh[1], Florian Klemme[1], Hussam

Industrial Session 1: AMS and RF Test

Room: Gaugain + Dali
Moderator:

Talk 1: A SystemC-AMS Development Framework for High Power IC Test-Hardware

Authors: Davide Turossi, Andrea Baschirotto
University of Milan Bicocca (IT)

Talk 2: Use UVM for AMS DFT through IEEE 1687 Procedural Description Language

Authors: Geert Seuren[1], Hitu Sharma[2], Rahul Lodwal[2]
[1]NXP Semiconductor (NL)
[2]NXP Semiconductor (IN)

Special Session 1: Reliability and Security of AI Hardware

Room: Van Gogh + Monet
Moderator: Marcello Traiola, Angeliki Kritikakou

Talk 1:

Speaker: Paolo Rech, University of Trento (IT)

Talk 2:

Speaker: Ernesto Sanchez Politecnico di Torino (IT)

Talk 3:

Speaker: Mehdi Tahoori, Karlsruhe Institute of Technology (DE)

Talk 4:

11:00 - 12:30 Parallel Sessions

Amrouch[1,2], Sybille Hellebrand[3], Hans-Joachim Wunderlich[1]
[1]University of Stuttgart (DE)
[2]Technical University of Munich (DE)
[3]University of Paderborn (DE)

Talk 3: Test Compression for Neuromorphic Chips

Authors: Xin-Ping Chen[1], Hsu-Yu Huang[1], Chu-Yun Hsiao[1], Shueh-Inn Hu[2], Chien-Mo Li[1]
[1]National Taiwan University (TW),
[2]Ming Chuan University (TW)

Talk 3: A Comprehensive Study on Improving Probe Card Transmission Lines for Effective High-Frequency Wafer-Level Testing

Authors: *Riccardo Vettori, Alessia Galli, Ivan Giudiceandrea*
Technoprobe (IT)

Speaker: *Russell Tessier, University of Massachusetts Amherst, US*

Talk 5:

Speaker: *Marcello Traiola, Inria Centre at Rennes University (FR)*

Talk 6:

Speaker: *Angeliki Kritikakou, University of Rennes (FR)*

12:30 – 14:00 Lunch Break

14:00 – 19:30 Afternoon Session

14:00 - 15:30 Parallel Sessions

Regular Session 2: AI in Test and Security

Room: A1
Moderator:

Talk 1: Detection of Stealthy Bitstreams in Cloud FPGAs using Graph Convolutional Networks (*Best Paper Award Candidate*)

Authors: *Jayeeta Chaudhuri, Krishnendu Chakrabarty*
Arizona State University (US)

Talk 2: Testing Spintronics Implemented Monte Carlo Dropout-

PhD Forum: PhD Forum Posters:

Room: Gaugain + Dali
Moderator:

Please check the PhD forum Poster sessions 1 and 2 for more details.

Special Session 2: Silent Data Corruption: Test or Reliability Problem?

Room: Van Gogh + Monet
Moderator: Bram Kruseman, NXP (NL)

Talk 1: Silent Data Corruptions at Scale

Speaker: *Harish Dixit*
Meta Platforms Inc (US)

Talk 2: Incompatible: Test Quality and Fortuitous Detection

Speaker: *Shawn Blanton*
Carnegie Mellon University (US)

14:00 - 15:30 Parallel Sessions

Based Bayesian Neural Networks

Authors: *Soyed Tuhin Ahmed[1], Kamal Danouchi[2], Michael Hefenbrock[3], Guillaume Prenat[2], Lorena Anghel[2], Mehdi Tahoori[1]*
[1]Karlsruhe Institute of Technology (DE)
[2]University of Grenoble Alpes, CEA, CNRS (FR)
[3]RevoAI GmbH (DE)

Talk 3: On-chip Built-In Self-Calibration of Thermal variations for Mixed-Signal In-Memory Computing

Authors: *Gaurav Singh[1], Omar Numan[1], Dipesh Monga[1], Martin Andraud[1,2], Kari Halonen[1]*
[1]Aalto University (FI)
[2]UC Louvain (BE)

Talk 3: Intermittent Silent Data Errors: Possible Physical Origins and Implications

Speaker: *Ben Kaczer IMEC (BE)*

15:30 – 16:15 Coffee Break - PhD Forum 1 and Industry Posters Room: Basement

PhD Forum Posters 1

Poster 1: On Parametrized Virtual Testing and Simulation of Verilog-AMS Behavioral Models

Authors: *Thorben Schey[1], Khaled Karoonlatifi[2], Andrey Morozov[1], Michael Weyrich[1]*
[1]University of Stuttgart (DE)
[2]Advantest Europe GmbH (DE)

Poster 2: Techniques for Building Reliable and Energy-Efficient Hardware Accelerators for Dynamic Deep Neural Networks

Authors: *Rama Kodamanchili, Maksim Jenihhin*
Tallinn University of Technology (EE)

Poster 5: Towards Ultra-Reliable Automotive Systems-on-Chip

Authors: *Giusy Iaria*

Poster 6: System-Level Test Techniques for Automotive SoCs

Authors: *Francesco Angione Politecnico di Torino (IT)*

15:30 – 16:15 Coffee Break - PhD Forum 1 and Industry Posters
Room: Basement

Poster 3: Design of efficient Hardware Inference Engines for Edge AI

Authors: *Ahsan Rafiq, Maksim Jenihhin*
Tallinn University of Technology (EE)

Poster 4: Deploying Compact and Dependable DNNs in Safety-critical Applications

Authors: *Leonardo Alexandrino De Melo[1], Alberto Bosio[1,2], Rodrigo Possamai Bastos[2]*
[1]Ecole Centrale de Lyon (FR)
[2]University Grenoble Alpes, CNRS (FR)

Poster 7: Leveraging FPGAs for Faster and Less Memory-Demanding Burn-In Testing

Authors: *Tommaso Foscale*
Politecnico di Torino (IT)

Poster 8: Exploiting The Connectivity Metric In Test Programs Generation

Authors: *Lorenzo Cardone*
Politecnico di Torino (IT)

Industrial Posters

Poster 1: Agile Methodologies applied to IC's testing

Authors: *Jey Nithyanandam, W Alban Haynse Immanuel, Jay Pankaj Shah, Khoushikh Sampath*
Infineon Technologies (US)

Poster 2: A Methodology on Validating the Vector DSP Processor in a Heterogeneous Microcontroller Using System Level-Notation

Authors: *Meghashyam Ashwathnarayan*
Infineon Technologies (IN)

Poster 3: Cross-talk aware Small Delay Defect Test with

Authors: *Dohan Lee*
Samsung Electronics Co (KR)

Poster 4: Automation of PMU module using POP for TTR

Authors: *Christina Kichenamourty, Jeyendran Nithyanadam, Sonia Kagale*
Infineon Technologies (IN)

Poster 5: Optimizing Digital Block Debug on ATE using Flat Pattern to Register Trace conversion

Authors: *Alban Haynse Immanuel, Jeyendran Nithyanadam, Jay Pankaj Shah, Khoushikh S*
Infineon Technologies (IN)

Poster 6: Adaptive Test Time Reduction for IoT devices in ATE

Authors: *Alban Haynse Immanuel, Jeyendran Nithyanadam,* Ragotham *Hari, Khoushikh S, Naveen S*
Infineon Technologies (IN)

16:15 - 17:45 Parallel Sessions

Regular Session 3: Design for Test and Trust

Room: A1
Moderator:

Industrial Sesson 2: Vendor Presentations

Room: Gaugain + Dali
Moderator:

Special Session 3: What Would Interactive Testing With 1687 Look Like?

Room: Van Gogh + Monet

16:15 - 17:45 Parallel Sessions

Talk 1: Test and Repair Improvement for UCIe (***Best Paper Award Candidate***)

Authors: *Tsung-Hsuan Wang[1,2], Po-Yao Chuang[1,3], Francesco Lorenzelli[1,4], Erik Jan Marinissen[1,5]*
[1]IMEC (BE)
[2]NYCU (TW)
[3]NTHU (TW)
[4]KU Leuven (BE)
[5]TU Eindhoven (NL)

Talk 2: IEEE 1838 Compliant Scan Encryption and Interity for 2.5/3D ICs

Authors: *Juan Suzano[1], Antoine Chastand[1], Emanuele Valea[2], Giorgio Di Natale[3], Anthony Philippe[2], Fady Abouzeid[1], Philippe Roche[1]*
[1]STMicroelectronics (FR)
[2]CEA-List (FR)
[3]TIMA (FR)

Talk 3: Design-for-Test for Intermittent Faults in STT-MRAMs

Authors: *Sicong Yuan[1,3], Mohammad Amin Yaldagard[1], Hanzhi Xun[1], Moritz Fieback[1], Erik Jan Marinissen[3], Woojin Kim[3], Siddharth Rao[3], Sebastien Couet[3], Mottaqiallah Taouil[1,2], Said Hamdioui[1,2]*
[1]Delft University of Technology (NL)
[2]CognitiveIC (NL)
[3]IMEC (BE)

Talk 1: The Advances in Shift-left Within DFT

Speaker: *Lee Harrison, Siemens Digital Industries Software (UK)*

Talk 2: Introducing Roguevation

Speaker: *Ric Dokken, Roguevation (US)*

Talk 3: DFT and Silicon Health Optimization with AI-Driven Test and Silicon Lifecycle Management

Speaker: *Yervant Zorian Synopsys (US)*

Moderators: *Michele Portolan (Grenoble-INP (FR)), Martin Keim (Siemens Digital Industries Software (US)), and Jeff Rearick (Siemens Digital Industries Software (CA))*

Speakers: *Hans Martin von Staudt (Renesas), Michele Portolan (Grenoble-INP), J-F Cote (Siemens EDA)*

18:00- 19:30 Pannel 1: Wine and Cheese Panel Room: A1

Wednesday May 22nd, 2024

08:30 – 12:30 Morning Session

Time	Room	Event	Session title and speaker
08:30 – 09:15	A1	Keynote 2 Chair:	***Sustainability and the Outlook of Semiconductor Industry*** *Cheng-Wen Wu – Southern Taiwan University of Science and Technology* (TW) **Abstract**: The environmental sustainability and global warming issues caused by the excessive and inappropriate consumption of the earth's resources by human beings have led to the goal of net-zero carbon emissions, which have been agreed by most countries in the world. The trends of electric vehicles, green energy, smart microgrid, etc., will change many industries in the future, including the semiconductor industry. In this talk, I will try to discuss the future development of the semiconductor industry that the ETS attendees may be concerned about from different perspectives, including quality and reliability of the products and systems.

09:15 - 10:15 Parallel Sessions

Regular Session 4: Analog and Mixed-Signal Test

Room: A1
Moderator:

Talk 1: Characterization of Ultra-low random jitter reduction methods up to 36 GHz

Authors: *David Keezer[1], Dany Minier[2], Hongjie Li[3]*
[1]Eastern Institute of Technology (CN),
[2]Boreas Technologies (CN)
[3]Tianjin University (CN)

Embedded Tutorial 1: Silent Data Corruptions (SDC) in Computing Systems: Early Predictions and Large-Scale Measurements

Room: Van Gogh + Monet
Moderator:

Speakers: *Dimitris Gizopoulos, University of Athens (GR) and Harish Dattatraya Dixit, Meta Platforms Inc (US)*

Embedded Tutorial 2: Lifetime Management of Embedded Memories

Room: Gaugain + Dali
Moderator:

Speakers: *Leticia Maria Bolzani Poehls, RWTH Aachen University (DE) and Moritz Fieback Delft University of Technology (NL)*

09:15 - 10:15 Parallel Sessions

Talk 2: Hierarchical Fault Simulation for Mixed-Signal Circuits Using Template Based Fault Response Modeling

Authors: *Tolga Aksoy[1], Nikhil Sagar Modala[1], Lakshmanan Balasubramanian[2], Rubin Parekhji[2], Sule Ozev[1]*
[1]Arizona State University (US)
[2]Texas Instruments (IN)

10:15 – 11:00 Coffee Break - PhD Forum 2 and McCluskey Posters Room: Basement

PhD Forum Posters 2

Poster 1: Improving the Effectiveness of Fuzz Testing by Incorporating Association Rule Mining for Hardware Verification

Authors: *Mohammad Reza Heidari Iman, Tara Ghasempouri*
Tallinn University of Technology (EE)

Poster 2: Manufacturing and In-Field Testing Techniques

Authors: *Gabriele Filipponi*
Politecnico di Torino (IT)

Poster 3: Time Guarantee and Reliable Execution for Safety-Critical Real-Time Systems

Authors: *Pegdwende Romaric Nikiema, Angeliki Kritikakou, Marcello Traiola, Olivier Sentieys*
Université de Rennes (FR)

Poster 4: Irradiation Tests: Deriving Memory Design Parameters

Poster 6: Exploring Side Channel Attacks on Cutting-Edge Adder-Free SRAM CIM

Authors: *Fouwad Mir, Abdullah Aljuffri, Mottaqiallah Taouil*
Delft University of Technology (NL)

Poster 7: Pre-Silicon Fuzzing of RISC-V Hardware Components and their Interactions

Authors: *Gijs Burghoorn, Abdullah Aljuffri, Mottaqiallah Taouil*
Delft University of Technology (NL)

Poster 8: Online Detection of Unique Faults in RRAMs

Authors: *Hanzhi Xun[1], Moritz Fieback[1], Mohammad Amin Yaldagard[1], Sicong Yuan[1], Hassen Aziza[2], Mottaqiallah Taouil[1,3], Said Hamdioui[1,3]*
[1]Delft University of Technology (NL)
[2]Aix-Marseille Université (FR)
[3]CognitiveIC (NL)

Poster 9: Reliability Assessment and Optimization of Dynamic DNNs for Edge Accelerators

10:15 – 11:00 Coffee Break - PhD Forum 2 and McCluskey Posters
Room: Basement

Authors: *Nima Kolahimahmoudi, Paolo Bernardi*
Politecnico di Torino (IT)

Authors: *georgios konstantinidis, maria k. Michael, Theocharis Theocharides*
University of Cyprus (CY)

Poster 5: A Novel Machine Learning-based Fault Shape Classification for Memories Embedded In Automotive Systems-on-Chip

Authors: *Giorgio Insinga, Paolo Bernardi*
Politecnico di Torino (IT)

McCluskey PhD Thesis Posters

Poster 1: Dependable Reconfigurable Scan Networks

Authors: *Natalia Lylina, Hans-Joachim Wunderlich*
University of Stuttgart (DE)

Poster 2: Toward Fault-Tolerant Applications on Reconfigurable Systems-on-Chip

Authors: *Corrado De Sio, Luca Sterpone*
Politecnico di Torino (IT)

Poster 3: SDfT: Secure Design for Testability

Authors: *Yogendra Sao, Sk Subidh Ali*
Indian Institute of Technology Bhilai (IN)

Poster 4: Design for Advanced Optical Test for Image and Photonic Sensors

Authors: *Julia Lefevre[1,2], Philippe Debaud[1], Patrick Girard[2], Arnaud Virazel[2]*
[1]STMicroelectronics (FR)
[2]LIRMM University of Montpellier/ CNRS (FR)

11:00 - 12:30 Parallel Sessions

Regular Session 5: *Reliability Analysis and monitoring*

Room: A1
Moderator:

Talk 1: Degradation Monitoring Through Software-controlled On-chip Sensors for RISC-V (Best Paper Award Candidate)

Authors: *Seyedehmaryam Ghasemi, Jonas Krautter, Tara Gheshlaghi, Sergej Meshkov,*

Industrial Sesson 3: *Memory Test*

Room: Van Gogh + Monet
Moderator:

Talk 1: Combining Built-In Redundancy Analysis with ECC for Memory Testing

Speaker: *Luc Romain[1], Paul-Patrick Nordmann[2], Benoit Nadeau-Dostie[1], Lori Schramm[3], Martin Keim[3]*
[1]Siemens Digital Industries Software (CA)

McCluksey Award: McCluksey PhD thesis candidates

Room: Gaugain + Dali
Moderators:

Candidate 1: Dependable Reconfigurable Scan Networks

Authors: *Natalia Lylina, Hans-Joachim Wunderlich*
University of Stuttgart

Candidate 2: Toward Fault-Tolerant

11:00 - 12:30 Parallel Sessions

Dennis R.E. Gnad, Mehdi Tahoori
Karlsruhe Institute of Technology (DE)

[2]Siemens Digital Industries Software (DE)
[3]Siemens Digital Industries Software (US)

Talk 2: Cross-Layer Reliability Analysis of NVDLA Accelerators: Exploring the Configuration Space

Authors: *Alessandro Veronesi[1], Alessandro Nazzari[2], Dario Passarello[2], Milos Krstic[1,3], Michele Favalli[4], Luca Cassano[2], Antonio Miele[2], Davide Bertozzi[5], Cristiana Bolchini[1]*
[1]IHP-Microelectronics (DE),
[2]Politecnico di Milano (IT),
[3]University of Postdam (DE)
[4]Universita' degli Studi di Ferrara (IT),
[5]University of Manchester (UK)

Talk 2: Semiconductor Application Fail Root Causes And Secure Test Remedy

Speaker: *Heguo Yin[1], Peter Poechmueller[2]*
[1]Shanndong University (CN)
[2]Neumonda GmbH (DE)

Applications on Reconfigurable Systems-on-Chip

Authors: *Corrado De Sio, Luca Sterpone*
Politecnico di Torino (IT)

Candidate 3: SDfT: Secure Design for Testability

Authors: *Yogendra Sao, Sk Subidh Ali*
Indian Institute of Technology Bhilai

Candidate 4: Design for Advanced Optical Test for Image and Photonic Sensors

Authors: *Julia Lefevre[1,2], Philippe Debaud[1], Patrick Girard[2], Arnaud Virazel[2]*
[1]STMicroelectronics (FR)
[2]LIRMM (FR)

Talk 3: CGAN-based Automated Fault Injection

Authors: *Troya Koylu, Cornelis Christiaan Berg, Praveen Vadnala*
Riscure BV (NL)

Talk 3: Power-Aware Test Scheduling for Memory BIST

Speaker: *Albert Au[1], Michal Kepinski[2], Artur Pogiel[2]*
[1]Siemens Digital Industries Software (CA)
[2]Siemens Digital Industries Software (PL)

12:30- 14:00 Pannel 1: Lunch

14:00 – 15:30 Afternoon Session

14:00- 15:30 Pannel 2 (Room-A1)

16:30- 22:00 Social Event

Thursday May 23rd, 2024

08:30 – 12:30 Morning Session

Time	Room	Event	Session title and speaker
08:30 – 09:15	A1	Keynote 3 Chair:	**It is All About Trust: The Road to Autonomous Driving Will Connect Test, Reliability and Safety** *Juergen Alt – Infineon Technologies* (DE) **Abstract**: At some point in the future, the majority of vehicles will be autonomous. When exactly that time will be, depends not only on technical availability but also on social acceptance. Confidence in such a technical system plays an essential, if not decisive, role. Already today, automotive semiconductors have high safety requirements as well as stricter quality and reliability targets than semiconductors supplied for consumer markets. This presentation will shed light on the challenges on the hardware side in the realization of semiconductor components for autonomous vehicles. The requirements on safety and reliability for the car of the future will increase. The measures already used today during manufacturing test, for Design-for-Test and for safety enablement need to be supplemented or replaced.

09:15 - 10:15 Parallel Sessions

Embedded Tutorial 3: Approximate Fault Tolerant Systems

Room: A1
Moderator:

Speakers: *Marcello Traiola[1], Alessandro Savino[2], and Alberto Bosio[3]*
[1]Rennes University (FR)
[2]Politecnico di Torino (IT)
[3]Ecole Centrale de Lyon (FR)

Embedded Tutorial 4: Silent Data Corruptions from Timing Marginalities Due to Process Variations

Room: Van Gogh + Monet
Moderator:

Speakers: *Adit Singh*
Auburn University (US)

Special Session 4: Test-Fleet Optimization Using Machine Learning

Room: Gaugain + Dali
Moderator: *Krishnendu Chakrabarty, Arizona State University (US)*

Speakers: *Dr. Andrew Dove (NI), Prof. Krishnendu Chakrabarty (Arizona State University)*

10:15 – 11:00 Coffee Break – Scientific and EU Projects Posters
Room: Basement

Poster 1: Modeling Thermal Effects For Biasing PUFs

Authors: *Aghiles Douadi[1], Elena Ioana Vatajelu[1], Paolo Maistri[1], David Hely[2], Vincent Beroulle[2], Giorgio Di Natale[1]*
[1]University of Grenoble Alpes, CNRS (FR)
[2]University of Grenoble Alpes (FR)

Poster 2: Post-Manufacture Criticality-Aware Gain Tuning of Timing Encoded Spiking Neural Networks for Yield Recovery

Authors: *Anurup Saha, Kwondo Ma, Chandramouli Amarnath, Abhijit Chatterjee*
Georgia Institute of Technology (US)

Poster 3: Extracting Weights of CIM-Based Neural Networks Through Power Analysis on Adder-Tree

Authors: *Fouwad Mir, Abdullah Aljuffri, Said Hamdioui, Mottaqiallah Taouil*
Delft University of Technology (NL)

Poster 4: Relation Coverage: A New Paradigm for Hardware/Software Testing

Authors: *Christoph Hazott, Daniel Grosse*
Johannes Kepler University (AT)

Poster 5: Optimizing System-Level Test Program Generation via Genetic Programming

Authors: *Denis Schwachhofer[1], Francesco Angione[2], Steffen Becker[1], Stefan Wagner[2,3], Matthias Sauer[4], Paolo Bernardi[2], Ilia Polian[1]*
[1]University of Stuttgart (DE)
[2]Politecnico di torino (IT)
[3]Technical University of Munich (DE)
[4]Advantest Europe (DE)

Poster 6: Scan Design Using Unsupervised Machine Learning to Reduce Functional Timing and Area Impact

Authors: Sandeep Kumar Goel[1], Ankita Patidar[1], Frank Lee[2]
[1]*TSMC (US)*
[2]TSMC (TW)

Poster 7: Assessing the Effectiveness of Software-Based Self-Test Programs for Static Cell-Aware Test

Authors: *Riccardo Cantoro[1], Michelangelo Grosso[2], Iacopo Guglielminetti[2], Reza Khoshzaban[1], Matteo Sonza Reorda[1]*
[1]Politecnico di Torino (IT)
[2]STMicroelectronics (IT)

Poster 8: AMS Test Stimulus Generation and Response Analysis Using Hyperdimensional Clustering: Minimizing Misclassification Rate

Authors: *Suhasini Komarraju, Mohamed Mejri, Akhil Tammana, Gowsika Dharmaraj, Chandramouli Amarnath, Abhijit Chatterjee*
Georgia Institute of Technology (US)

Poster 9: Transcoders: A Better Alternative to Denoising Autoencoders

Authors: *Pushpak Raj Gautam, Alex Orailoglu*
UC San Diego (US)

11:00 - 12:30 Parallel Sessions

Regular Session 6: Hardware Security

Room: Gaugain + Dali
Moderator:

Talk 1: Power Analysis Attack Against post-SAT Logic Locking Schemes

Authors: *Nassim Riadi[1], Florent Bruguier[1], Pascal Benoit[2], Sophie Dupuis[1], Marie-Lise Flottes[1]*
[1]LIRMM (FR)
[2]Universite de Montpellier (FR)

Talk 2: A Novel Power Analysis Attack against CRYSTALS-Dilithium Implementation

Authors: *Yong Liu[1], Yuejun Liu[1], Yongbin Zhou[1,2], Yiwen Gao[1], Zehua Qiao[2], Huaxin Wang[1]*
[1]Nanjing university of science and technology (CN)
[2]Chinese Academy of Sciences (CN)

Talk 3: Counteracting Rowhammer by Data Alternation

Authors: *Stefan Lung[1], Georgi Gaydadjiev[1], Said Hamdioui[1,2], Mottaqiallah Taouil[1,2]*
[1]Delft University of Technology (NL)
[2]Cognitive IC (NL)

Industrial Sesson 4: What will be required to effectively test processors, high end SoC or chiplet: will we need new DFT, a lot of silicon sensor data or applying more SLT?

Room: A1
Moderator: *Matteo Sonza Reorda Polito*

Panelists: *Nir Sever[1], Ric Dokken[2], Dave Armstrong[3]*
[1]Proteantecs
[2]Roguevation
[3]Advantest

Special Session 5: Testing for Reliability of Modern Power Electronic Components

Room: Van Gogh + Monet
Moderators: Francesco Iannuzzo

Talk 1: Reliability challenges on next-generation film capacitors for power electronic applications

Authors: *Thomas Ebel*
University of Southern Denmark (DK)

Talk 2: Testing for abnormal conditions of modern power electronic devices

Authors: *Francesco Iannuzzo*
AAU Energy, Aalborg University (DK)

Talk 3: Innovative testing techniques for bond-wire fatigue in power electronic components

Authors: *Golta Khatibi*
Institute for Chemical Technologies and Analytics, TU Wien (AT)

Talk 4: Accelerated life testing of power electronic components: how far are we?

Authors: *Zoubir Khatir*
SATIE Laboratory, French Institute of Science and Technology for Transport, Development and Networks (FR)

12:30- 14:00 Lunch

14:00 – 16:30 Afternoon Session

14:00 - 15:30 Parallel Sessions

Regular Session 7: Test and Verification in Emerging Circuits

Room: A1
Moderator:

Talk 1: Fault Sensitivity Analysis of Printed Bespoke Multilayer Perceptron Classifiers

Authors: *Priyanjana Pal[1], Florentia Afentaki[1,2], Haibin Zhao[1], Gurol Saglam[1], Michael Hefenbrock[3], Georgios Zervakis[2], Michael Beigl[1], Mehdi Tahoori[1]*
[1]Karlsruhe Institute of Technology (DE)
[2]University of Patras (GR)
[3]RevoAI GmbH (DE)

Talk 2: Polynomial Formal Verification of Approximate Adders with Constant Cutwidth

Authors: *Mohamed Nadeem[1], Chandan Kumar Jha[1], Rolf Drechsler[1]*
[1]University of Bremen (DE)
[2]DFKI (DE)

Industrial Sesson 5: Reliability and Test Development

Room: Gaugain + Dali
Moderator: *Matteo Sonza Reorda*
Politecnico di Torino (IT)

Talk 1: Hardware-independent ATE Software for SLT

Authors: *Ric Dokken*
Roguevation Inc (US)

Talk 2: In-chip Monitoring for Extended Reliability Testing and Mission Profile Monitoring Feedback Loop

Authors: *Andrea Matteucci[1], Luca Moriconi[2]*
[1]ProteanTecs (IL)
[2]ELES (IT)

Talk 3 Virtual Test Development Using Pre-Silicon Verification Environment

Authors: *Ryan Ignacio, Ernst Aderholz, Quint Atol, Bernhard Baptist, Waseem Bharah, Rainer Holzner,*

Special Session 6: IEEE Std P3405: New Standard-under-Development for Chiplet Interconnect Test and Repair

Room: Van Gogh + Monet
Moderators: *Saket Kumar Goyal – Broadcom (USA)*

Talk 1: Requirements for Chiplet Interconnect Repair and Analysis of Legacy Solutions

Authors: *Adrian Evans*
CEA/LIST (FR)

Talk 2: Chiplet Interconnect Repair Logic Description with Google's Protocol Buffers

Authors: *Po-Yao Chuang and ErikJan Marinissen*
IMEC (BE)

Talk 3: How IEEE Std P3405 Enables EDA Interoperability

Authors: *Martin Keim*
Siemens Digital Industries Software (US)

14:00 - 15:30 Parallel Sessions

Vinayak Kamanuri, Andras Kun, Keyue Ma, Bruno Mariacher, Otto Pfabigan, Adam Przybilla, Darko Samardzic, Florian Schlagbauer, Mario Schleicher, Patrick Valiente, K-Ee Vinod, Otmar Zikulnig, Enzo Vargas
Infineon Technologies (DE)

15:30- 16:00 Conference Closing and Student Awards

16:00- 16:30 Coffee Break (Basement)

16:30 - 18:30 Parallel Workshop Sessions

AI-TREATS Workshop

Room: Rembrandt
Program Chairs:
Annachiara Ruospo[1], Haralampos-G. Stratigopoulos[2]
[1]Politecnico di Torino (IT)
[2] Sorbonne Université (FR)

CiTaR Workshop

Room: Van Gogh
General Chair: Erik Jan Marinissen, IMEC (BE)

Program Chair: Martin Keim
Siemens Digital Industries Software (US)

eARTS Workshop

Room: Gaugain
General Chairs: Yervant Zorian[1], Davide Appello[2,]
[1]Synopsys (US)
[2]Technoprobe (IT)

Program Chirs: Riccardo Cantoro[1], Wim Dobbelaere[2]
[1]Politecnico di Torino (IT)
[2]Onsemi (BE)

18:00- 19:30 Social Event: Welcome Reception

Friday May 24th, 2024

08:30 – 15:30 Morning Session

08:30 - 15:30 Parallel Workshop Sessions

AI-TREATS Workshop

Room: Rembrandt
Program Chairs:
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